The counting and the enable circuits control DC similarly to UC. Only two changes occur in the counting method. The accumulated value is reset and held at the preset value instead of 0000, and the count is decreased, not increased, by one when the counting circuit changes from non-conducting to conducting. The actual value is held at the preset value if enable is non-conducting. The count decreases on transition of the count input when the enable circuit is conducting.

Again, the count is stored in the actual register. Counting begins at the preset value, constant or variable. The coil is energized and its contacts are operated when the count reaches 0000. The count remains at 0000 until the enable circuit stops conducting.

Note

If preset is held in a register and set to zero, the coil will be ON, regardless of the state of the enable or count circuit (i.e., preset = 0 = actual).

SPECIFICATIONS

PRESET

UC is preset at the value at which the coil energizes.

DC is preset at the value at which down counting begins.

This value may be a constant (0000 through 9999) or it may be held in a Holding Register (HR), Input Register (IR), or Output Register (OR). The value is 1 through 65535 if it is held in a register.

ACTUAL

The current value is held in:

- Holding Register (HR)
- Output Register (OR)

COIL

In the up count, the coil is energized when actual is greater than or equal to preset.

In the down count, the coil is energized when actual equals zero.

UC/DC TRUTH TABLE

See Table 1.

APPLICATIONS

In the shared register counter application (see Fig. 2), UC determines the actual value of DC. The DC function appears first in the program. If IN0002 is closed, both counters are active. When IN0001 is closed, HR0002 increments by one and continues to increment every time IN0001 is opened and closed. If IN0003 is opened and closed, the contents of HR0002 are decremented by one and continue to decrement until 0000 is reached. This circuit could be used to keep track of products entering and leaving a production line, as shown in Figure 3.

TABLE 1. UC/DC TRUTH TABLE

Enable Circuit	Count Circuit	UC Result	DC Result
0	0	Actual is held at zero.	Actual is held at preset.
0	↑	Actual is held at zero.	Actual is held at preset.
0	1	Actual is held at zero.	Actual is held at preset.
1	0	Actual is held at current value.	Actual is held at current value.
1	↑	Counter increments.	Counter decrements.
1	1	Actual is held at current value. **Note** When actual equals preset, the counter continues past preset.	Actual is held at current value. **Note** When actual equals zero, the counter stops.

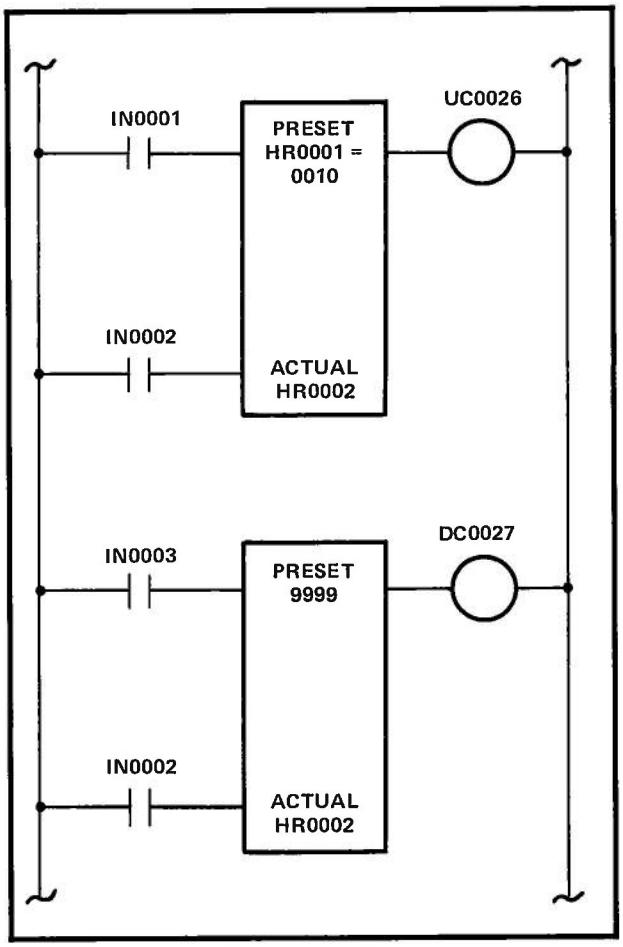

Figure 2. Shared Register Counter

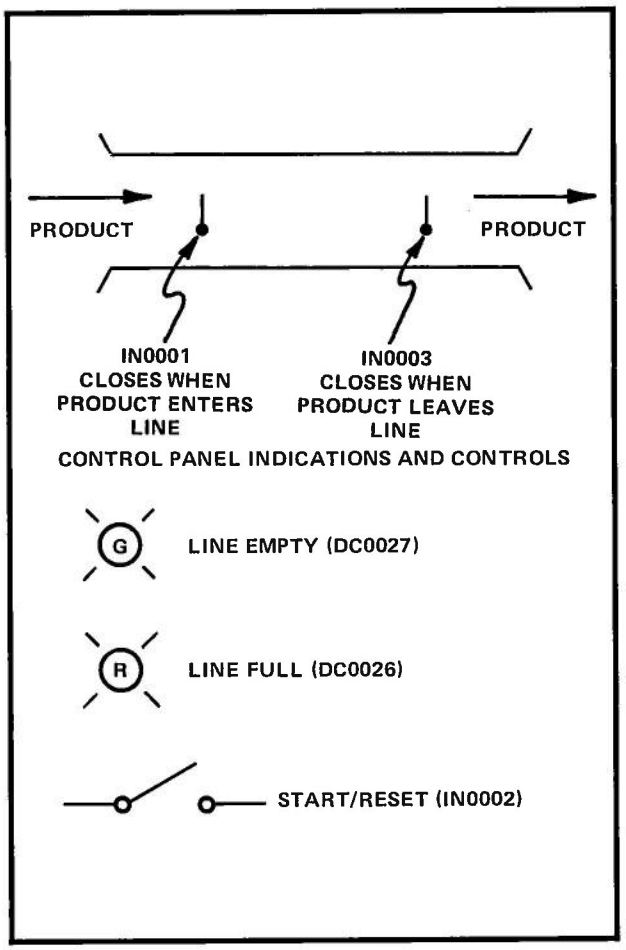

Figure 3. Shared Counter Application

UI — I/O UPDATE IMMEDIATE

DESCRIPTION

The I/O Update Immediate (UI) function updates the status of registers or groups when the UI function is executed in the logic scan, in addition to normal I/O update at the end of the logic scan. Energizing a UI enable input updates the status of the specified input register or group and its corresponding output register or group. De-energizing a UI enable input stops the update routine. UI function symbology is shown in Figure 1.

CAUTION

DO NOT use the NL-744 Multiplexed Register Input module or the NL-754 Multiplexed Register Output module when the UI function is used to update register pairs.

Note

The UI function is programmed only with the NLPL-780 or NLPL-780P CRT Program Loaders, software version number 3.0 or greater.

SPECIFICATIONS

OPERATING DATA

The designation specifies the I/O pair for updating. This can be a pair of single registers or a group. One of the following may be used:

- IR: Input Register/Output Register
- IG: Input Group/Output Group

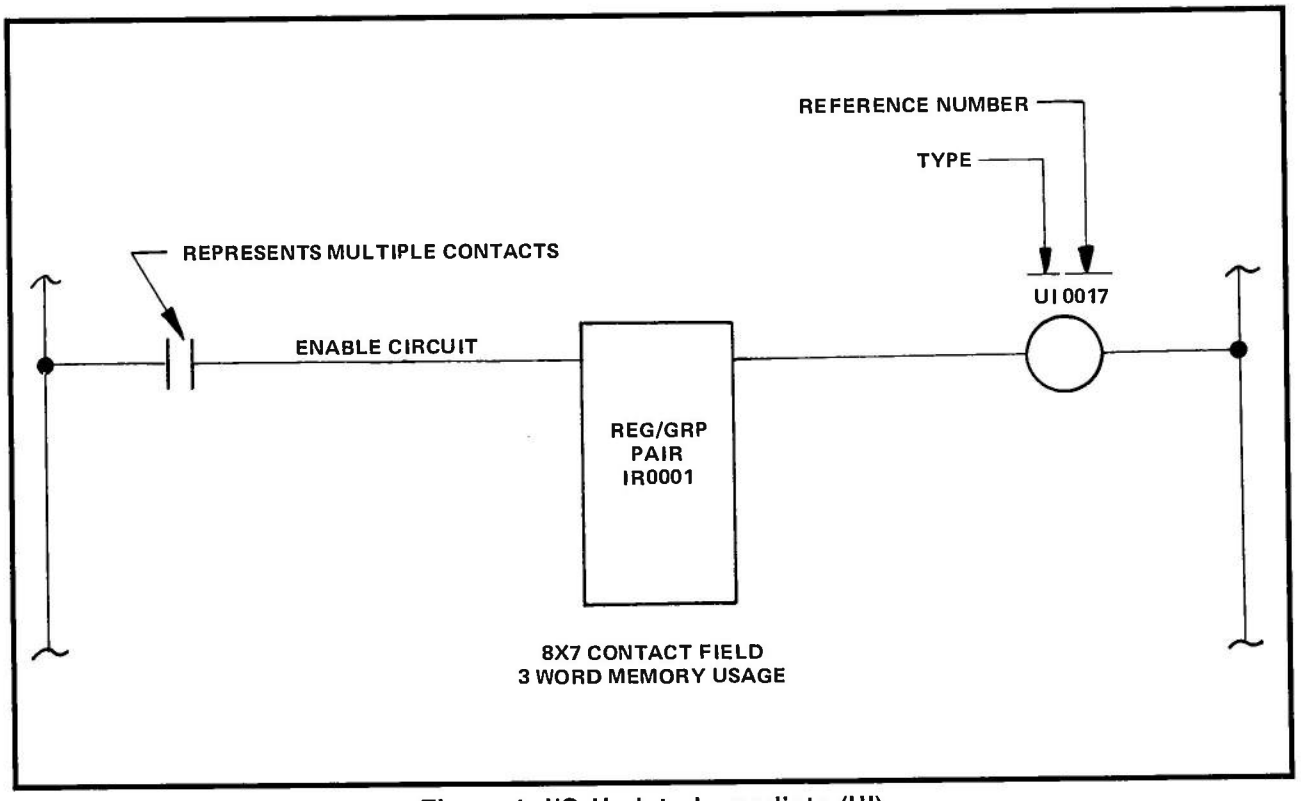

Figure 1. I/O Update Immediate (UI)

ENABLE CIRCUIT

When conducting, the enable circuit energizes the UI function, and the specified pair of I/O registers or groups are updated. When not conducting, the enable circuit de-energizes the UI function and no immediate updating occurs during the logic scan.

COIL

When the coil is energized, the specified pair of I/O registers or groups is updated immediately. When the coil is de-energized, no updating occurs.

APPLICATIONS

The UI function can be used to periodically monitor the status of critical inputs. For example, if the user wants output GE0037 (CR0037) to activate immediately when IR0006 is greater than or equal to 1024, the program shown in Figure 2 can be repeatedly programmed at appropriate intervals throughout the ladder program. The coil UI0126 has no meaning to the UI function and can be duplicated, saving coils for other uses.

EXECUTION ORDER

UI0126 is always ON when GE0037 is executed. If GE0037 is not turned ON, UI0126 is turned OFF for remainder of the scan.

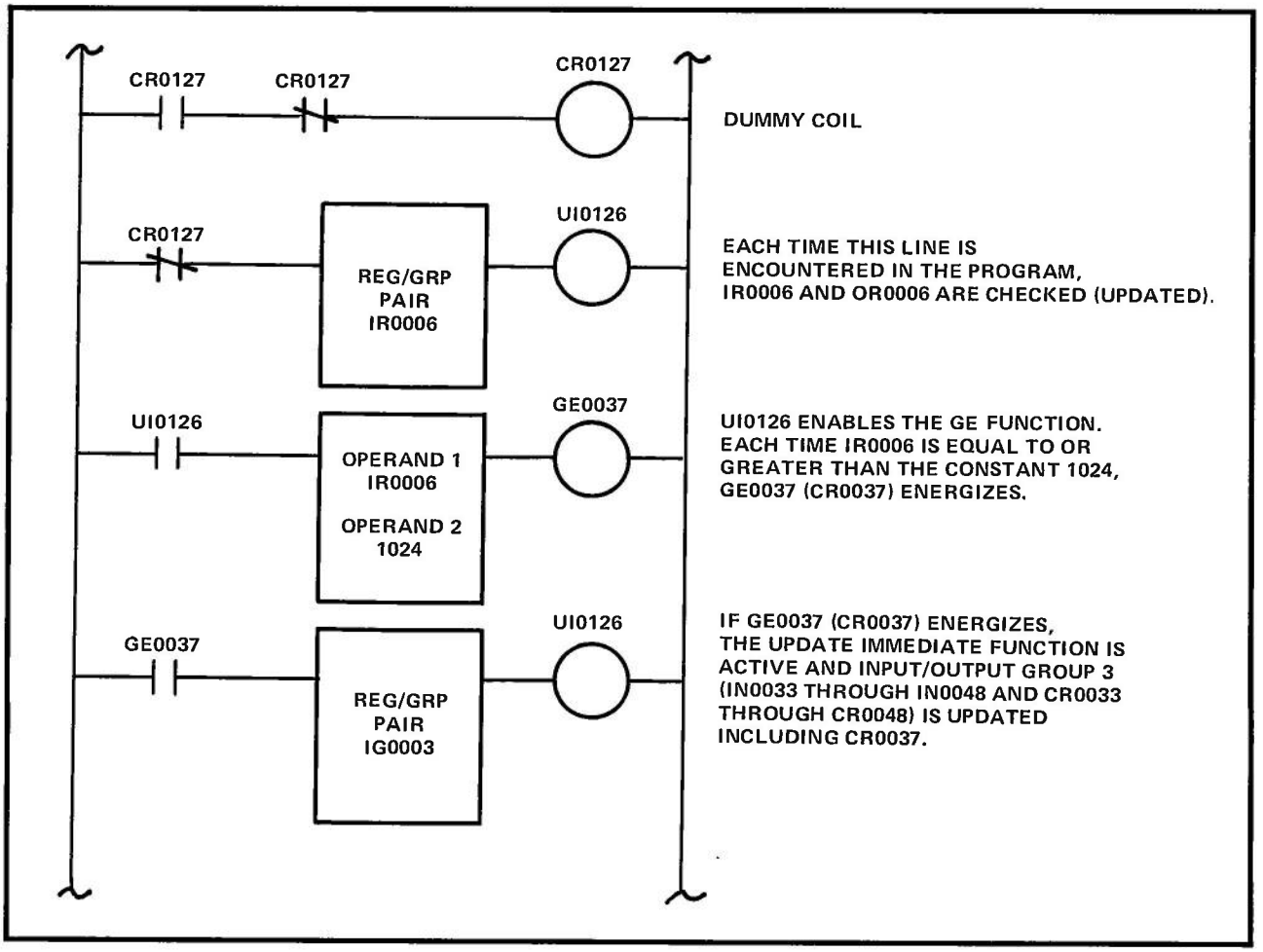

Figure 2. UI Operations

US — UPDATE SELECT

DESCRIPTION

The Update Select (US) function allows the user to specify the number of quarters of I/O that are updated at the end of a processor scan. The scan rate is effectively increased by eliminating the time spent updating unused I/O quarters. This function also updates portions of I/O at a much slower scan rate. US function symbology is shown in Figure 1.

SPECIFICATIONS

OP CODE 25

The Op Code defines the Literal (LT) as the US function.

I/O QUARTERS

A constant value determines the number of I/O quarters to be updated when the function is enabled. Table 1 lists the quarters and the updated groups.

TABLE 1. I/O QUARTERS

I/O Quarter	I/O Updated
1	I/O Group 1
2	I/O Groups 1 and 2
3	I/O Groups 1, 2, and 3
0 or 4 +	All I/O is updated.

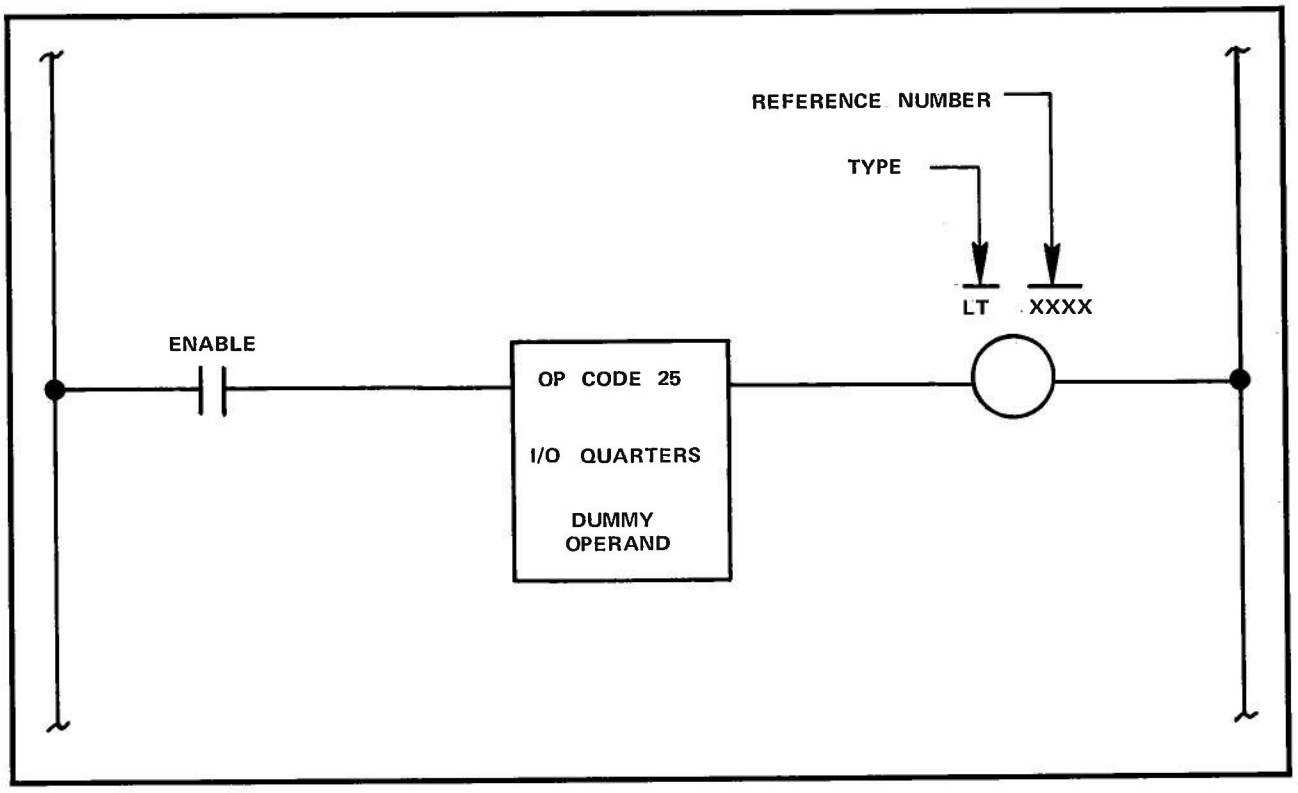

Figure 1. Update Select (US)

Dummy Operand

The dummy operand is a constant value of 1 to complete the special function.

US TRUTH TABLE

See Table 2.

TABLE 2. US TRUTH TABLE

Enable	Result
0	The coil is de-energized and all I/O is updated.
1	The coil is energized and the specified I/O quarters are updated.

APPLICATIONS

If the user has a program whose inputs and outputs are in Group 1 only (Discrete Inputs 1 through 64, Discrete Outputs 1 through 64, Input Registers 1 through 8, Output Registers 1 through 8), the US function allows only Group 1 to be updated, increasing the processor scan rate. The program segment in Figure 2 shows this operation. US always enables, allowing only Group 1 to update.

If some portions of I/O are not as critical as others, update frequency is arranged accordingly. The ladder diagram in Figure 3 shows this operation. The self-resetting timer, TT0001, energizes for one scan every 10 seconds. I/O Groups 1 and 2 (Discrete I/O 1 through 128, and Input and Output Registers 1 through 16) update every scan. All I/O updates every 10 seconds.

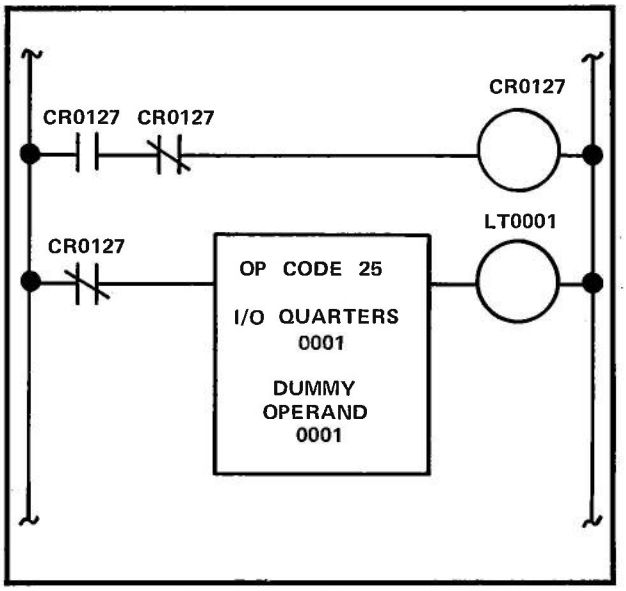

Figure 2. US Program

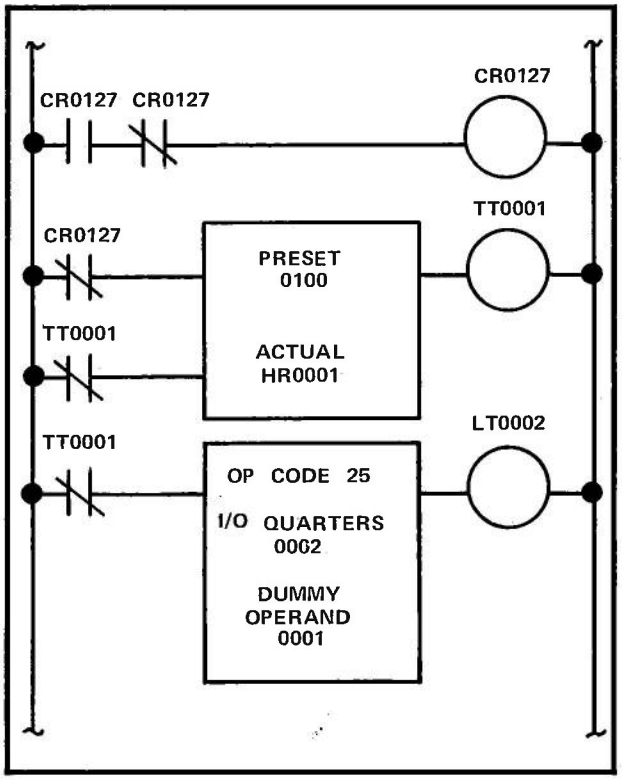

Figure 3. US for I/O at Differing Rates

XM — XOR MATRIX

DESCRIPTION

The XOR Matrix (XM) function exclusively OR's the contents of a pair of matrices on a bit-per-bit basis; then, it places the result in a destination matrix location. XM function symbology is shown in Figure 1.

The XM operation occurs when the enable circuit changes from non-conducting to conducting. The original pair of matrices is unaffected by the operation. See Table 1.

TABLE 1. XM TRUTH TABLE SAMPLE

Matrix 1 Bit N	Matrix 2 Bit N	Destination Matrix Bit N
0	0	0
0	1	1
1	0	1
1	1	0

Note
N is the same bit in all three matrices.

SPECIFICATIONS

COIL

The coil energizes when the enable circuit is conducting and the result of the operation is non-zero.

OP CODE 88

The Op Code defines the Literal (LT) as XM.

Note

When the software changes allow, LT becomes XM.

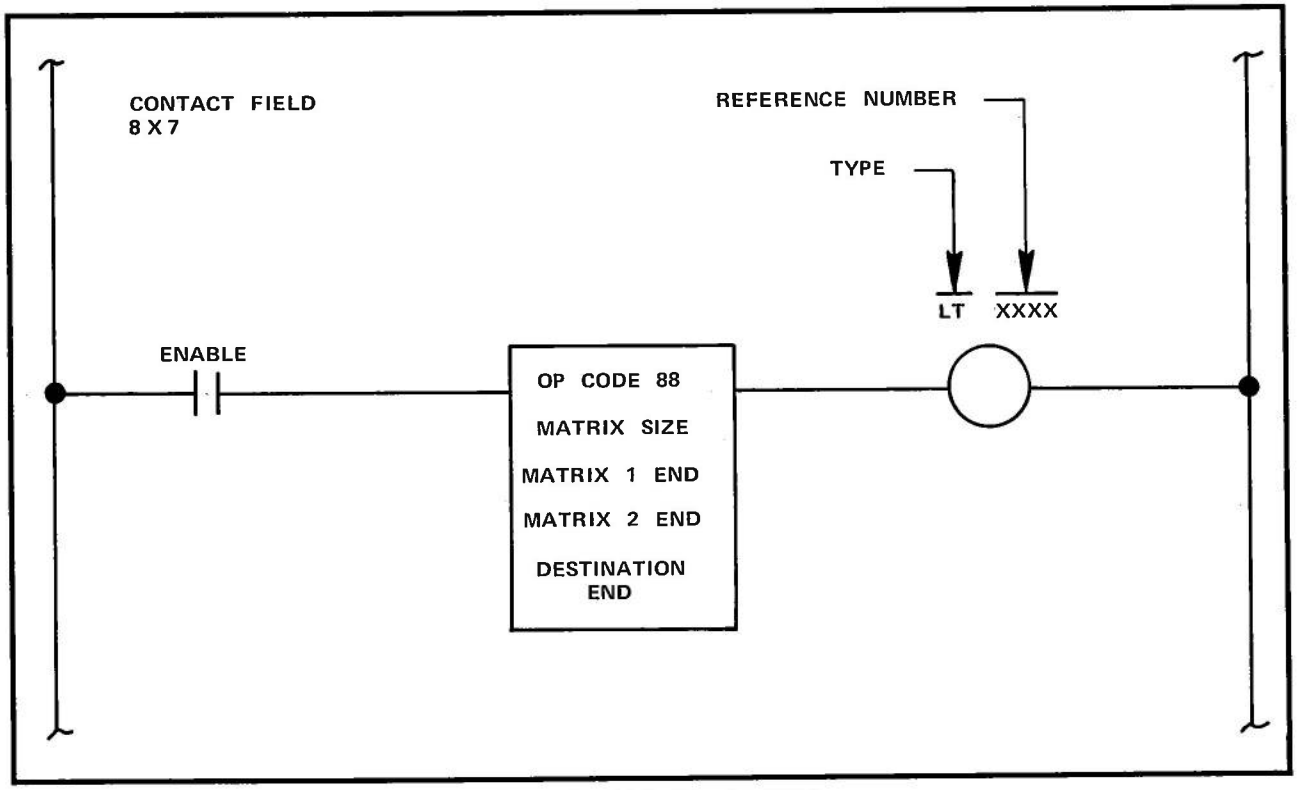

Figure 1. XOR Matrix (XM)

MATRIX SIZE

The matrix size is a constant value that defines the number of registers included in the matrix. The range is 1 through 128, which is subject to the limitations listed under Matrices 1 and 2 in Table 2.

Note

The highest number holding register is limited by and dependent upon the memory size.

MATRIX 1/MATRIX 2 END

Matrix 1/Matrix 2 end defines the type and number of the last register in Matrix 1 and Matrix 2 that will be OR'ed. The type and number are limited as indicated in Table 2.

TABLE 2. XM END REGISTERS

Type	Limit
HR	⩽ 1792
IR	⩽ 32 (PC-700) ⩽ 8 (PC-900A) ⩽ 16 (PC-900B)
OR	⩽ 32 (PC-700) ⩽ 8 (PC-900A) ⩽ 16 (PC-900B)
IG	⩽ 16 (PC-700) ⩽ 8 (PC-900 A/B)
OG	⩽ 32 (PC-700) ⩽ 8 (PC-900A) ⩽ 16 (PC-900B)

DESTINATION END

The destination end defines the type and number of the last register in the matrix containing the results of the XM function. The type and number limitations are shown in Table 3.

XM TRUTH TABLE

See Table 4.

APPLICATIONS

The XM function is used to make desired state versus actual state comparisons. If the actual state is equal to the desired state, the coil is de-energized when the enable circuit is conducting. If the actual state does not equal the desired state, the coil is energized with the enable circuit conducting. See Figure 2.

TABLE 3. XM DESTINATION END REGISTER

Type	Limit
HR	⩽ 1792
OR	⩽ 32 (PC-700) ⩽ 8 (PC-900A) ⩽ 16 (PC-900B)
OG	⩽ 32 (PC-700) ⩽ 8 (PC-900A) ⩽ 16 (PC-900B)

TABLE 4. XM TRUTH TABLE

Enable	Result
0	The coil is de-energized. Matrix 1, Matrix 2, and the destination remain unchanged.
↑	XOR's Matrix 1 with Matrix 2, placing the results in the destination. The coil energizes if the result is non-zero, and de-energizes if the result is zero.
1	The coil, as indicated above, results in the destination matrix.

The ladder diagram for the XM function is shown in Figure 3. When IN0001 changes from open to closed, the XM function occurs. If IN0001 remains closed, the coil gives the following indications:

Energized = Matrix 1 ≠ Matrix 2
De-energized = Matrix 1 = Matrix 2

Figure 4 shows an example of a pair of matrices that are exclusively OR'ed.

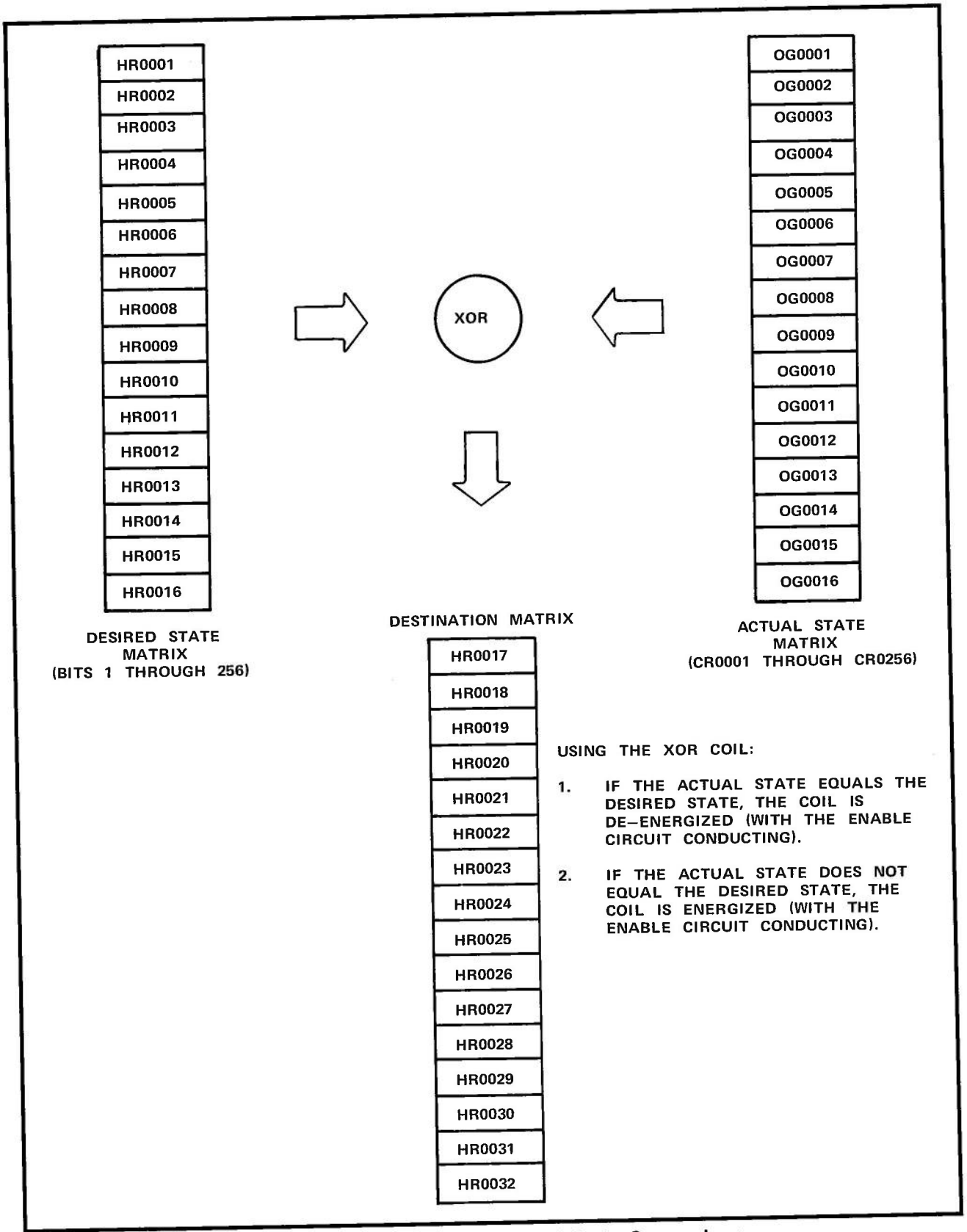

Figure 2. Desired State vs. Actual State Comparison

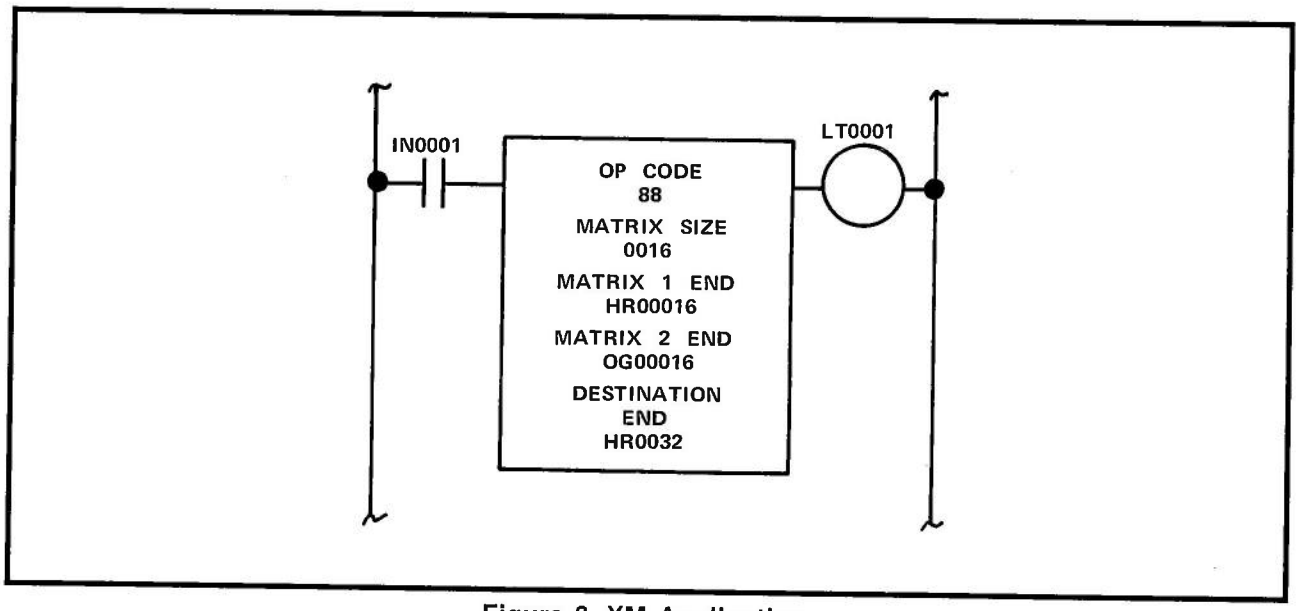

Figure 3. XM Application

MATRIX 1

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
HR0001	1	0	0	1	0	1	0	0	1	1	1	1	0	0	1	1

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
HR0002	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33
HR0003	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

MATRIX 1 END

MATRIX 2

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
HR0004	0	1	1	0	0	0	0	0	0	0	1	0	1	1	0	0

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
HR0005	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33
HR0006	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

MATRIX 2 END

DESTINATION MATRIX

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
OG0001	1	1	1	1	0	1	0	0	1	1	0	1	1	1	1	1

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
OG0002	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33
OG0003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DESTINATION END

Figure 4. A Pair of Exclusively OR'ed Matrices