

APPENDIX A. GLOSSARY

- ADDRESS*** - An identification as represented by a name, label, or number for a register, location in storage, or any other data source or destination such as the location of a station in a communications network.
- ANALOG SIGNAL** - A continuous signal that depends directly on magnitude (voltage or current) to represent some condition. For example, a voltage could represent the speed of a motor (e.g., 5 V corresponding to 200 rpm; 10 V corresponding to 400 rpm, etc.).
- ANALOG-TO-DIGITAL CONVERTER** - A circuit that converts a continuous signal that depends directly on magnitude to a discrete signal that represents magnitude by a coded number. For example: a 0 through 10 V signal can be represented by a set of binary signals whose numerical values from 0 through 4095 are proportional to the voltage (e.g., 0 V = 0, 5 V = 2048, 10 V = 4095).
- BAUD** - The measure of the number of bits per second that can be transmitted in a data communications system.
- BCD** - An abbreviation for Binary Coded Decimal. BCD is a system of representing decimal data in binary code. For example: in BCD, 16 is represented as 0001 (for 1) and 0110 (for 6).
- BINARY** - A numbering system that uses a base number, or radix, of two. There are two digits (1 and 0) in the binary system.
- BIT** - An acronym for Binary digIT. A bit can assume one of two possible states: ON or OFF; high or low; logic 1 or logic 0; etc.
- BIT CLEAR** - A special function that clears a bit in a holding register or an output register. When a Bit Clear (BC) coil is energized, the designated bit is cleared to a logic 0. When the BC coil is de-energized, the designated bit is unaffected.
- BIT FOLLOW** - A special function coil that, when energized, sets the bit for which the Bit Follow (BF) is programmed. When a BF coil is de-energized, the designated bit clears to a logic 0.

*Definitions taken from the IEEE Standard Dictionary of Electrical and Electronics Terms, 2nd edition, by permission of the Institute of Electrical and Electronics Engineers.

BIT PICK - A contact used to determine the state of individual bits in registers.

BIT SET - A Special function that sets a bit in a holding register or an output register. When a Bit Set (BS) coil is energized, the designated bit is set to a logic 1. When a BS coil is de-energized, the designated bit is unaffected.

BUS* - One or more conductors used for transmitting signals or power from one or more sources to one or more destinations.

CHAIN - To program two or more functions as a group so that the group operates as a single function with expanded capabilities. For example, drum controllers may be chained to expand the number of steps beyond the individual 128 step maximum.

CLOCK - A device that generates periodic signals for synchronization or timing.

CMOS - An abbreviation for Complimentary Metal Oxide Semiconductor. A family of very low-power, high-speed integrated circuits used in the PC-1100/1200.

CONDUCTING - A contact circuit is conducting whenever there is a complete path of conduction from the left side to the right side of the circuit.

CONTACT AREA - The area available for contact circuits when programming a function. The width of the area indicates the number of series contacts allowed from left to right. The height of the area indicates the number of parallel paths allowed.

CONTACT CIRCUIT - A contact circuit is a collection of normally open (NO) and/or normally closed (NC) contacts connected in series and/or in parallel and attached to a coil or a special function block.

CPU - An abbreviation for Central Processing Unit; used interchangeably with processor.

CRT - The abbreviation for Cathode Ray Tube, which is an electronic display tube similar to the familiar TV picture tube. A CRT is used as the display screen on the program loader.

DATA - Information (e.g., the state of a device, or the contents of a register).

DESTINATION - The location of data after the completion of an operation. For example, after two numbers are added, the destination is a holding register in which the result is placed.

DIGITAL SIGNAL - A discrete signal or set of signals that depends on the presence or absence of some quantity (e.g., voltage, current, etc.) to represent some condition. Digital signals are often combined into sets that can be interpreted as numbers. For example, binary voltages (either 0 or 5 VDC) in sets of four (XXXX) can represent the numbers 0 thru 15 using the binary system.

DISCRETE INPUTS OR OUTPUTS - Individual inputs or outputs providing one signal and operating according to a single bit of information (as opposed to register inputs or outputs, which when regrouped, provide 16 signals and operate according to 16 bits of information).

ENABLE - A circuit that allows a function or operation to be activated.

EXECUTIVE PROGRAM - In the processor, the executive program is a set of coded instructions, programmed by the manufacturer, that controls the monitoring of inputs, the solving of the user's ladder diagram program, and the updating of the output states.

FORCE - A mode of operation in the program loader that allows the operator (as opposed to processor) to control the state of a contact.

INPUT CIRCUIT - An input circuit is a real-world device (e.g., limit switch, transducer, computer register, etc.), its associated wiring, and the input module point to which it is connected. The input module's function is to convert field voltage levels (e.g., 5 V, 12 V, 120 V, etc.) into proper processor signal levels.

I/O - An abbreviation for Input/Output. For example, a group of input modules and output modules might be referred to as I/O modules.

I/O UPDATE IMMEDIATE - A special function that, when enabled, causes a register pair or input/output (I/O) group to be updated immediately upon the execution of a special function, as well as at the end of the processor scan.

INTERFACE - A device that transmits data between two subsystems that often cannot be directly wired together.

LABEL - The means by which registers, coils, and contacts are identified. Each label consists of two parts: the type and the reference number. For example, the label assigned to a holding register may be HR0115.

LADDER DIAGRAM - A complete control scheme normally drawn as a series of contact circuits and coils arranged between two vertical control supply lines so that the horizontal lines of contacts appear similar to rungs of a ladder. A ladder diagram is normally the reference document used by the operator when entering the control program.

LATCH - A device that continues to store the state of the input signal after the signal is removed. The input state is stored until the latch is reset. Latches are created using the Bit Set, Bit Clear, and Bit Pick functions.

LINE - A circuit or group of circuits together with the associated coil and/or special function block. (See Figure A-1).

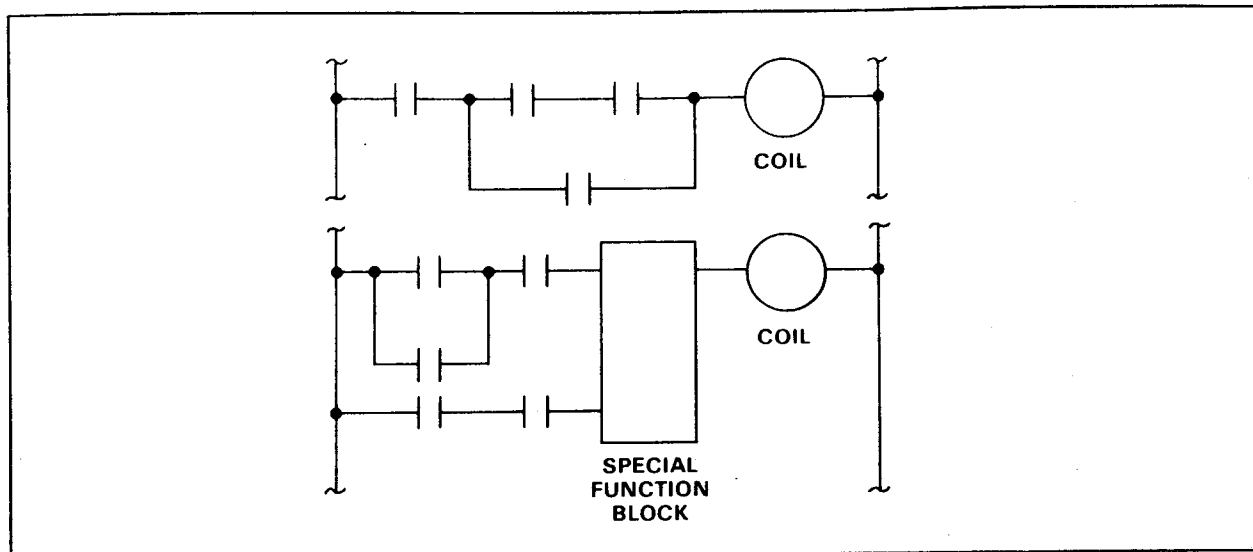


Figure A-1. Typical Circuit Lines

LITERAL - A special function format reserved for the programming of all future special functions.

LOAD - To place data (e.g., a ladder diagram) into the processor's memory.

LOGIC COIL - A coil, associated with a control relay or special function, that is not used to operate a real-world output circuit.

LOGIC 1 - See the definition for bit.

LOGIC 0 - See the definition for bit.

MEMORY* - A device in which data can be entered; in which it can be held; and from which it can be retrieved.

MODULE* - Any assembly of interconnected components which constitutes an identifiable device, instrument, or piece of equipment. A module can be disconnected, removed as a unit, and replaced with a spare. It has definable performance characteristics which permit it to be tested as a unit. A module can be a printed circuit board or subassembly of a larger device, provided it meets the requirements of this definition.

MONITOR - The process of determining the state or condition of an input, a coil, or a register.

MULTIPLEX - To carry out multiple functions in an independent but related manner. Multiplexing often involves interleaving or otherwise combining several signals so that they may be handled by a single device.

NODE - A common connection point between two or more contacts or elements in a circuit. (See Figure A-2).

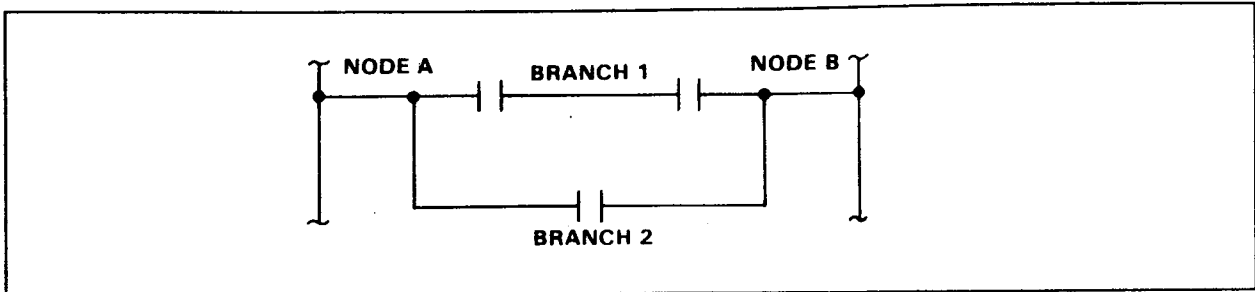


Figure A-2. Branch 1 in Parallel with Branch 2

NOISE ENERGY REJECTION - The specialized circuitry that prevents voltage spikes, RFI, transients, and other electrical noise found in a typical industrial environment from causing any undesired operation.

NON-CONDUCTING - A contact circuit is non-conducting whenever there is not a complete path of conduction from the left side to the right side of the circuit.

NORMALLY CLOSED - Abbreviated NC. It is the designation applied to a relay contact that is closed when the coil of the relay is not energized; an input contact that is closed when its associated input converter is not activated; or a Bit Pick contact that is closed when its associated bit in a register is a logic 0.

NORMALLY OPEN - Abbreviated NO. It is the designation applied to a relay contact that is open when the coil of the relay is not energized; an input contact that is open when its associated input converter is not activated; or a Bit Pick contact that is open when its associated bit in a register is a logic 0.

OFFLINE PROGRAMMING - A method of programming that is done with the processor stopped and all outputs turned OFF.

ONLINE PROGRAMMING - A method of programming by which rungs in the program may be inserted, changed or deleted while the processor is running and controlling outputs under program control.

OPERAND - 1) Either of the two numbers used in a basic computation to produce an answer. For example, in the computation $2 \times 3 = 6$, 2 and 3 are the operands. 2) Data required for the operation of a special function.

OUTPUT CIRCUIT - An output module point, real-world device (e.g., motor starter, digital readout, panel meter, etc.), and its associated wiring. The output module's function is to convert processor signal levels to field voltage levels that are used by real-world devices.

OUTPUT COIL - A coil, associated with a control relay or special function, which is used to operate an output circuit. Output coils are used with those lines that must directly operate output circuits. (See the definition for logic coil.)

PARALLEL - In a coil circuit, parallel refers to two or more branches connected between the same pair of nodes. (See Figure A-2.)

PICK - To select the state of a particular register bit.

PRESET - The time or count limit established for a timer or an up counter. When this limit is reached, the associated coil is activated. In a down counter, the preset is the value at which the counter begins and to which it is reset.

PROCESSOR - The part of the programmable controller that performs logic solving, program storage, and special functions within a programmable controller system.

REFERENCE NUMBER - 1) A number used to designate a particular coil. For example, reference numbers 0001 thru 0128 may designate outputs coils. 2) A number used to designate a particular input circuit, input register, holding register, or output register. (See the definition for label.)

REGISTER - A location in memory used for the storage of data in the form of a multi-bit number. In Numa-Logic programmable controllers, there are three types of registers:

- Input Register (IR)

Input registers accept and store data from register input modules.

- Output Register (OR)

The data stored in the output registers is available from register output modules.

- Holding Registers (HR)

Holding registers typically store intermediate processor results. Data in these registers is not directly accessible from register I/O modules.

(See the definition for discrete inputs or outputs.)

RS-232-C - An Electronic Industries Association (EIA) standard for serial data transfer. Westinghouse programmable controllers have RS-232-C port(s) for data communication from the processor to program loader, or with a computer.

RS-485 - An Electronic Industries Association (EIA) standard for serial data transfer. Some Westinghouse programmable controllers, such as the PC-1100/1200, have RS-485 port(s) for data communication from the processor to program loader, or with a computer.

SCAN - The scanning operation, as performed by the processor, is the sequential examination of both the ladder diagram instructions stored in memory and the status of inputs, outputs, and registers to determine whether or not to energize or de-energize each coil, or perform the desired special functions.

SCAN TIME - The time required to make one complete scan through memory and to update the status of all inputs and outputs.

SERIES - In a coil circuit, series refers to two or more adjacent contacts connected to each other. (See Figure A-3.)

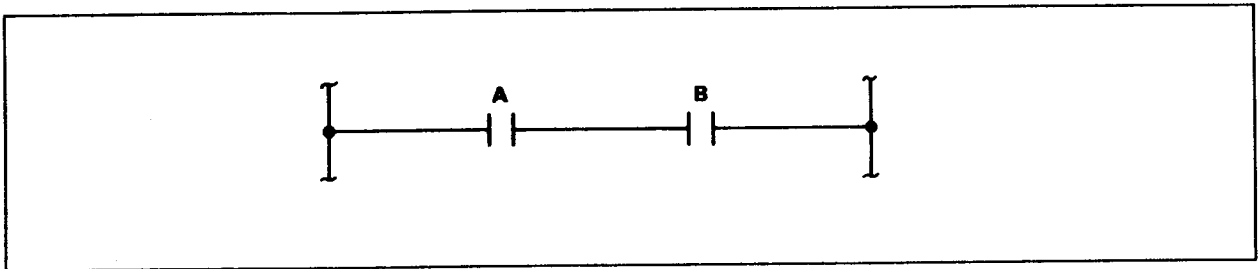


Figure A-3. Contact A in Series with Contact B

SOURCE - In special functions (e.g., the Move [MV] function and the Binary to Decimal [BD] function), the source is the place of origin for the data that is to be moved or converted. A source may be a register or a group of discrete inputs/outputs.

STORE/STORAGE - To retain information in a device from which it can later be withdrawn.

TRANSFER - The process of moving data from one device, module, or register over one or more data lines to another device, module, or register; the process of moving data from input to output.

TTL - An abbreviation for Transistor-to-Transistor Logic. A family of low-voltage, low-power integrated circuits used in Westinghouse components.

TYPE - A two-letter designation used to specify a function, an input, a register, or an output. (See the definition for label.)

WORD - An ordered sequence of bits treated as one unit.

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APPENDIX B. CONTROLLER SPECIFICATIONS

This appendix summarizes the specifications of the PC-1100 and -1200 controllers. For additional details on the controllers and other system components, refer to Section 2.

TABLE B-1. PC-1100/1200 SPECIFICATIONS

Item	PC-1100 Specification	PC-1200 Specification
Power		
AC line voltage (nominal)	120 or 240 VAC	120 or 240 VAC
Input voltage range (AC)	102 to 132 VAC or 187 to 253 VAC	102 to 132 VAC or 187 to 253 VAC
Frequency (nominal)	50/60 Hz	50/60 Hz
Power Requirement	75 VA maximum	75 VA maximum
Optional DC power	24 VDC nominal (20 to 28 VDC range)	Not available
Timing		
Scan rate	7 msec per 1000 contacts (typical)	0.7 msec per 1000 contacts (typical)
Update time (full I/O bus)	3 msec	9.87 msec (can be reduced using Update Select function)
I/O Update Immediate function (typical)	170.0 μ (OFF) 480.0 μ (ON)	55.0 μ (OFF) 204.0 μ (ON)
I/O Types		
	Discrete and/or register	Discrete and/or register

TABLE B-1. PC-1100/1200 SPECIFICATIONS, CONT'D

Item	PC-1100 Specification	PC-1200 Specification
<p align="center">Memory</p> <p>User memory</p> <p>Type</p>	<p>0.5, 1.5, 2.5, or 3.5 K words</p> <p>CMOS RAM (16-bit words)</p>	<p>2, 4, 8, or 16 K words</p> <p>CMOS RAM (16-bit words)</p>
<p align="center">Memory Backup</p> <p>Battery type and quantity</p>	<p>3 type AA alkaline (Catalog No. NLB-1100)</p>	<p>1 type AA (3.5 V) lithium 1800 mAh nominal capacity (Catalog No. NLB-1200)</p>
<p align="center">Communications Ports</p> <p>Serial Port A</p> <p>Serial Port B</p>	<p>RS-232</p> <p>RS-232 or RS-485 (Advanced PC-1100 only)</p>	<p>RS-232</p> <p>RS-232 or RS-485</p>
<p align="center">Environmental</p> <p>Ambient operating temperature</p> <p>Relative humidity</p>	<p>0 to 60° C (32 to 140° F)</p> <p>0 to 90%, non-condensing through 0 to 60° C range</p>	<p>0 to 60° C (32 to 140° F)</p> <p>0 to 90%, non-condensing through 0 to 60° C range</p>
<p align="center">Dimensions</p> <p>Controller</p> <p>NLR-1004 Main Rack</p> <p>NLR-1008 Main Rack, NLRE-1009/1011/1011B Expansion Rack</p> <p>NLR-1012 Main Rack, NLRE-1013 Expansion</p> <p>NLR-1016 Main Rack NLRE-1017 Expansion</p> <p>Required enclosure depth</p>	<p>11.75 (h) X 5.75 (d) X 5.25 in. (w)</p> <p>11.75 (h) X 11.38 (w)</p> <p>11.75 (h) X 17.50 (w) (NLRE-1009 only)</p> <p>Not applicable</p> <p>Not applicable</p> <p>8 in. with key in place 6 in. without key</p>	<p>11.75 (h) X 5.75 (d) X 5.25 in. (w)</p> <p>11.75 (h) X 11.38 (w)</p> <p>11.75 (h) X 17.50 (w)</p> <p>11.75 (h) X 23.65 (w)</p> <p>11.75 (h) X 29.775 (w)</p> <p>8 in. with key in place 6 in. without key</p>

TABLE B-1. PC-1100/1200 SPECIFICATIONS, CONT'D

Item	PC-1100 Specification	PC-1200 Specification
Applicable Standards ¹		
Noise Susceptibility	Meets NEMA standards as specified in ISC 3-304	Meets NEMA standards as specified in ISC 3-304
Surge	IEEE surge withstand test as specified in STD 472-1974	IEEE surge withstand test as specified in STD 472-1974
Safety	Designed to CSA standards; UL listed.	Designed to CSA standards; UL listed.

¹ Standards listed are for the PC-1100/1200 controller unit. All I/O modules and racks are designed to UL standards (certification pending). To determine additional standards which apply to individual I/O modules, refer to the applicable Instruction Leaflets.

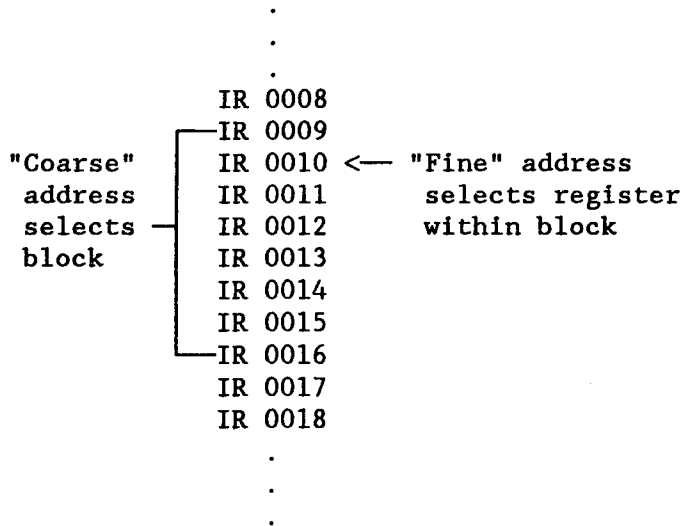


APPENDIX C. MODULE ADDRESSING DETAILS

This appendix provides information on address switch settings for analog, register, and 16-point discrete I/O modules. For a general discussion of 1000 Series I/O addressing, and for information on 8-point discrete module addressing, refer to Paragraph 3-15.

The module address for analog, register, and 16-point modules is set using DIP switches on the back of the module. These DIP switches may also set other variables (such as high/low = true). The number of switches and their settings are not the same for all modules, so it is important to refer to the module-specific information on the pages which follow.

Typically, the address setting will consist of two parts: "coarse" and "fine". In general, the "coarse" address refers to a block of registers, while the "fine" address selects the position of a single register within the block. For example, to set the card address IR 0010, the coarse address setting would designate the block IR 0009-0016, and the fine address setting would select the second register within the block:



For the PC-1250 only, the selected address may be on the High bus or Low bus. As described in Paragraph 3-15, the High bus address can be considered an offset of the Low bus address. This offset is always 8 for IG/OG or 64 for IR/OR. Since the High/Low bus selection is made at the main rack NL-1077 module, not the I/O module, the switch settings at the module are the same for both buses. For example, the same DIP switch settings will be used to select IR 0001 or IR 0065.

The following pages provide specific switch settings for each of the following analog, register, and 16-point modules:

- NL-1017 Register Input Module
- NL-1018 Register Output Module
- NL-1045, -1046, -1049, and -1050
Eight-bit Analog Input Modules
- NL-1052 Twelve-bit Analog Input Module
- NL-1057 Eight-bit Analog Output Module
- NL-1030F 24VDC Discrete Input Module and
NL-1060F 24VDC Discrete Output Module

NL-1017 Register Input Module

Ten-position DIP switch at the back edge of the module determines addressing and module operation.

- SW 1 LVS - Latch or zero data (Up/Down) on external power supply failure
- SW 2 High/Low (Up/Down) Strobe Selection
- SW 3 High/Low (Up/Down) True Selection
- SW 4 IG/IR (Up/Down) Selection - Determines section of the Controller's I/O image (IG or IR) in which the module's data will be placed. ²
- SW 5 Coarse address - Selects one block of eight Registers within
6 the block of 64 Registers (per bus)
7
- SW 8 Fine address - Selects Register within a block of eight Registers
9
10

Coarse Address - Block Selection

SW			IR Block	
5	6	7	Low Bus	High Bus ¹
0	0	0	1 - 8	65 - 72
0	0	1	9 - 16	73 - 80
0	1	0	17 - 24	81 - 88
0	1	1	25 - 32	89 - 96
1	0	0	33 - 40	97 - 104
1	0	1	41 - 48	105 - 112
1	1	0	49 - 56	113 - 120
1	1	1	57 - 64	121 - 128

²

Fine Address - Register Selection

SW			IR/IG
8	9	10	Reg. within group
0	0	0	1st
0	0	1	2nd
0	1	0	3rd
0	1	1	4th
1	0	0	5th
1	0	1	6th
1	1	0	7th
1	1	1	8th

0 = Up , 1 = Down (with respect to Module PC board)

- ¹ High bus addresses available for PC-1250 only. High and low buses are addressed the same. Physical location within high bus maps to controller's I/O image with an offset of 64 for Registers or 8 for Groups.
- ² For IG addressing, leave coarse addressing at base setting (shown above as 'IR Block 1-8'). At most, eight input groups are available per bus.
- ³ For the PC-1100, valid addresses are IR 1-8 and IG 1-4.
For the PC-1200-xxx0, valid addresses are IR 1-32 and IG 1-4.
For other PC-1200 models, valid addresses are IR 1-64 and IG 1-8.
For the PC-1250, valid addresses are IR 1-128 and IG 1-16.

NL-1018 Register Output Module

Ten-position DIP switch at the back edge of the module determines addressing and module operation.

- SW 1 Fine address - Selects Register within a block of eight Registers
 2
 3
- SW 4 Coarse address - Selects one block of eight Registers within
 5 the block of 64 Registers (per bus)
 6
- SW 7 High/Low (Up/Down) True Selection
- SW 8 OG/OR (Up/Down) Selection - Determines section of the Controller's I/O
 image (OG or OR) in which the module's data will be placed. ²
- SW 9 For Future use - Leave in Up position
 10

Coarse Address - Block Selection

SW			OR Block	
4	5	6	Low Bus	High Bus ¹
1	1	1	1 - 8	65 - 72
0	1	1	9 - 16	73 - 80
1	0	1	17 - 24	81 - 88
0	0	1	25 - 32	89 - 96
1	1	0	33 - 40	97 - 104
0	1	0	41 - 48	105 - 112
1	0	0	49 - 56	113 - 120
0	0	0	57 - 64	121 - 128

0 = Up, 1 = Down (with respect to Module PC board)

Fine Address - Register Selection

SW			OR/OG
1	2	3	Reg. within group
1	1	1	1st
0	1	1	2nd
1	0	1	3rd
0	0	1	4th
1	1	0	5th
0	1	0	6th
1	0	0	7th
0	0	0	8th

¹ High bus addresses available for PC-1250 only. High and low buses are addressed the same. Physical location within high bus maps to controller's I/O image with an offset of 64 for Registers or 8 for Groups.

² For OG addressing, leave coarse addressing at base setting (shown above as 'OR Block 1-8'). At most, eight input groups are available per bus.

³ For the PC-1100, valid addresses are OR 1-8 and OG 1-4.
 For the PC-1200-xxx0, valid addresses are OR 1-32 and OG 1-4.
 For other PC-1200 models, valid addresses are OR 1-64 and OG 1-8.
 For the PC-1250, valid addresses are OR 1-128 and OG 1-16.

NL-1045, -1046, -1049, -1050 Eight-bit Analog Input Modules

Six-position DIP switch at the rear of the module determines starting address for a sequential group of two Registers (for the NL-1045 or -1049) or four Registers (for the NL-1046 or -1050).

- SW 1** For future use - Leave in Up position.
- SW 2** Coarse starting address - Selects one block of eight Registers
3 within the block of 64 Registers (per bus).
4
- SW 5** Fine starting address - Selects Register within a block of eight
6 Registers

Coarse Starting Address

SW				IR Block	
1	2	3	4	Low Bus	High Bus ¹
0	0	0	0	1 - 8	65 - 72
0	0	0	1	9 - 16	73 - 80
0	0	1	0	17 - 24	81 - 88
0	0	1	1	25 - 32	89 - 96
0	1	0	0	33 - 40	97 - 104
0	1	0	1	41 - 48	105 - 112
0	1	1	0	49 - 56	113 - 120
0	1	1	1	57 - 64	121 - 128

0 = Up, 1 = Down (with respect to Module PC board)
 X = Don't Care

Fine Starting Address

SW		NL-1045, -1049
5	6	Starting Address ²
0	0	1st Register
0	1	3rd Register
1	0	5th Register
1	1	7th Register

SW		NL-1046, -1050
5	6	Starting Address ²
0	X	1st Register
1	X	5th Register

- ¹ High bus addresses available for PC-1250 only. High and low buses are addressed the same. Physical location within high bus maps to controller's I/O image with an offset of 64 for Registers or 8 for Groups.
- ² For IG addressing, leave coarse addressing at base setting (shown above as 'IR Block 1-8'). At most, eight input groups are available per bus.
- ³ For the PC-1100, valid addresses are IR 1-8 and IG 1-4.
 For the PC-1200-xxx0, valid addresses are IR 1-32 and IG 1-4.
 For other PC-1200 models, valid addresses are IR 1-64 and IG 1-8.
 For the PC-1250, valid addresses are IR 1-128 and IG 1-16.

NL-1052 Twelve-bit Analog Input Module

A four-position DIP switch at the rear of the module selects a sequential group of eight Input Registers (one Register per analog channel). The module configuration is set using switches underneath the module lens. As an aid to the user, the lens on this module incorporates several charts showing compressed addressing and module set-up information.

By sliding the lens up about two inches, the addressing information and the rear DIP switches can be viewed simultaneously. The addressing switches are described below.

The front lens can be removed by sliding it upward. When the lens is removed, the module configuration DIP switches are accessible. Using these switches, each of the eight channels (out of the selected block of eight) can be individually deselected. When an address is deselected in this way, it is available for use by another module. Module set-up information is presented in a compressed format on the back of the lens.

SW 1 Select the Register address range
 2
 3

SW 4 For future use - Leave in Up position.

Block setting

SW		IR Block			
1	2	3	4	Low Bus	High Bus ¹
0	0	0	0	1 - 8	65 - 72
1	0	0	0	9 - 16	73 - 80
0	1	0	0	17 - 24	81 - 88
1	1	0	0	25 - 32	89 - 96
0	0	1	0	33 - 40	97 - 104
1	0	1	0	41 - 48	105 - 112
0	1	1	0	49 - 56	113 - 120
1	1	1	0	57 - 64	121 - 128

0 = Up, 1 = Down (with respect to Module PC board)

¹ High bus addresses available for PC-1250 only. High and low buses are addressed the same. Physical location within high bus maps to controller's I/O image with an offset of 64 for Registers or 8 for Groups.

² For the PC-1100, only valid addresses are IR 1-8
 For the PC-1200-xxx0, valid addresses are IR 1-32.
 For other PC-1200 models, valid addresses are IR 1-64.
 For the PC-1250, valid addresses are IR 1-128.

NL-1057 Eight-bit Analog Output Module

Ten position DIP switch at the rear of the Module determines addressing and module operation. A separate DIP switch at the bottom of the module sets output ranges. (See NL-1057 Instruction Leaflet for range selection and general operation.)

- SW 1 Pack/Unpack Mode (Up/Down).
- SW 2 Low/High Byte Selection (Up/Down) - Unpack mode only.
- SW 3 LVS - Latch or zero data (Up/Down) on external power supply failure, Controller fault, or keyswitch Stop
- SW 4 Coarse starting address - Selects one block of eight Registers
5
6 within the block of 64 (per bus).
- SW 7 Fine starting address - Selects starting Register of a sequential
8 group of two or four Registers (depending on pack or unpack mode selection).
- SW 9 For future use - Leave in Up position.
10

Coarse Starting Address

SW			OR Block	
4	5	6	Low Bus	High Bus ¹
0	0	0	1 - 8	65 - 72
0	0	1	9 - 16	73 - 80
0	1	0	17 - 24	81 - 88
0	1	1	25 - 32	89 - 96
1	0	0	33 - 40	97 - 104
1	0	1	41 - 48	105 - 112
1	1	0	49 - 56	113 - 120
1	1	1	57 - 64	121 - 128

Fine Starting Address

SW		Pack Mode
7	8	Starting Address
0	0	1st Register
0	1	3rd Register
1	0	5th Register
1	1	7th Register

SW		Unpack Mode
7	8	Starting Address
0	X	1st Register
1	X	5th Register

0 = Up, 1 = Down (with respect to Module PC board)
X = don't care

¹ High bus addresses available for PC-1250 only. High and low buses are addressed the same. Physical location within high bus maps to controller's I/O image with an offset of 64 for Registers.

² For the PC-1100, valid addresses are OR 1-8.
For the PC-1200-xxx0, valid addresses are OR 1-32.
For other PC-1200 models, valid addresses are OR 1-64.
For the PC-1250, valid addresses are OR 1-128.

NL-1030F 24VDC Discrete Input Module
NL-1060F 24VDC Discrete Output Module

A four plus one position DIP switch at the back edge of the module determines addressing range and type. Earlier modules (without the "F" suffix), which have only four DIP switches for addressing, do not allow Register addressing.

SW 1 Select the Register or Group address range
2
3
4

SW 5 Group/Register (Up/Down) - Determines section of the Controller's I/O image (IG/IR for NL-1030F or OG/OR for NL-1060F) in which the module's data will be placed.

SW				Low Bus		High Bus ¹	
1	2	3	4	R/G	Discrete Ref.	R/G	Discrete Ref.
1	1	1	1	1	1 - 16	9	129 - 144
0	1	1	1	2	17 - 32	10	145 - 160
1	0	1	1	3	33 - 48	11	161 - 176
0	0	1	1	4	49 - 64	12	177 - 192
1	1	0	1	5	65 - 80	13	193 - 208
0	1	0	1	6	81 - 96	14	209 - 224
1	0	0	1	7	97 - 112	15	225 - 240
0	0	0	1	8	113 - 128	16	241 - 256

0 = Up, 1 = Down - With respect to the PC board

¹ High bus addresses available for PC-1250 only. High and low buses are addressed the same. Physical location within high bus maps to controller's I/O image with an offset of 64 for Registers or 8 for Groups.